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# ASCI PathForward Project



# PathForward Project



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# PathForward Project Team

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# A PathForward Strategy

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Build future high end computing systems from building blocks (hardware and software) created to address the commodity computing marketplace.

- concentrate investments (which are small compared to the commodity marketplace R&D) very carefully in those areas (hardware and software) which will enable commodity systems to be scaled-up to satisfy high-end computing requirements



# PathForward Project

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"Establish multi-year development and engineering efforts to create the critical integrating and scaling technologies required for balanced computing environments at the scale of 10 to 30 TeraFLOPS (TFLOPS) in the late 1999 to 2001 timeframe."



# Balanced “Ultra-Scale” Computing

- ◆ Balanced systems at 10 -100 TFLOPS scale place stringent requirements on the internode interconnect, I/O and storage subsystems, distributed system software, and programming environment.
- ◆ ASCI balanced systems ratios (hardware):
  - 1 TeraFLOPS peak performance /
  - 1 Terabyte memory size / 50 Terabyte disk storage /
  - 16 Terabyte per second cache bandwidth / 3 Terabyte per second memory bandwidth /
  - 0.1 Terabyte per second I/O bandwidth / 10 Gigabyte per second disk bandwidth /
  - 1 Gigabyte per second archival storage bandwidth /
  - 10 Petabyte archival storage.

In scaling up over several orders of magnitude, these requirements will be difficult to achieve.



# PathForward Project: Development and Engineering Opportunities



- ◆ To achieve balanced, high-end, scientific computing at 10 TFLOPS and beyond,
- ◆ that can be made available on a time scale sufficiently rapid to impact future ASCI platform and subsystem procurements--notably 30 TFLOPS in the 2001 timeframe,
- ◆ that will accelerate extended capabilities of commercial product lines to market, and
- ◆ will not be created by commercial market forces in the time scale of interest.



# PathForward has a strategic focus



- ◆ extends beyond enhancement of existing platforms
- ◆ should impact multiple ASCI applications
- ◆ seeking widest possible impact on ASCI systems
  - ◆ software usable on multiple platforms
  - ◆ hardware impact on multiple generations





# PathForward Critical Technology Areas



- ◆ Finite Phase 1 funding limits our current scope to the most critical technologies
- ◆ Critical technology areas were identified in a preliminary exercise
- ◆ These are documented in the PathForward Project Description
- ◆ This is available at  
<http://www.llnl.gov/ascii-pathforward>



# PathForward

## Critical Technology Areas



- ◆ **Scaleable High-Performance Interconnects**
- ◆ **Distributed Parallel Operating System Software**
- ◆ **Parallel Scaleable Programming Environment**
- ◆ **Ultra-Scale, High-Performance Storage**



# ASCI hardware requirements



Level	Effective Latency (CPU cycles)	Bandwidth (Random read/write)	Size
On-chip cache**, L1	2-3 ●	16-32 B/cycle ●	$10^{-4}$ B/flop * ● ↑
Off-chip cache**, L2 (SRAM)	5-6 ●	16 B/cycle ●	$10^{-2}$ B/flop * ● ↑
Local main memory (DRAM)	30-80 (15-30) ↓	2-8 B/flop pk (2-8 B/flop sustained) ↓	1 B/flop ● ↑
“nearby nodes”	300-500 (30-50) ↓	1-8 B/flop (8 B/flop) ↓	1 B/flop ●
“far away nodes”	1000 (100-200) ↓	1 B/flop (1 B/flop) ↓	1 B/flop ●
I/O (memory disk)	10 ms ●	0.01-0.1 B/flop ●	10-100 B/flop ●
Archive (disk-tape)	Seconds ●	$10^{-4}$ B/flop (0.001-0.01 B/flop) ↓	$10^2$ B/flop $10^4$ B/flop ↓
User access	1/10 s (1/60 s)	OC3/desktop (OC12-48 /desktop) ↓	100 users ●
Multiple sites	1/10 s ●	●	●

Compute engine

Interconnect

Primary investment priority

Secondary investment priority

1996-1998 Situation  
(1998-2000 Requirements)

Industry Trend



Industry gets better at meeting requirements



Industry gets worse at meeting requirements



Industry continues to meet requirements

\* Equivalent integer and floating-point data calculation rates are required.

\*\* Cacheless systems with equivalent performance are fully acceptable.



# ASCI software requirements



	Security	Scalability	Functionality & Performance	Portability
Human/Computer Interface	↑ Δ	↓ Δ	Visualization ↓ Δ	↑ ●
Visualization	↑ Δ	↓ Δ	Internet ↑ Δ	↑ ●
Internet technology	↑ ●	↓ Δ	↓ Δ	↑ Δ
Application Environment	↑ ●	↓ Δ	↓ Δ	↑ Δ
Programming Environment				
— programming model	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— libraries	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— compilers	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— debuggers	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— performance tools	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— object technologies	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— scientific data	↓ Δ	↓ Δ	↓ Δ	↓ Δ
Management				
Distributed Operating software				
— I/O	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— file systems	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— storage systems	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— reliability	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— network	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— comm systems	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— systems admin	↓ Δ	↓ Δ	↓ Δ	↓ Δ
— distributed resource mgmt	↓ Δ	↓ Δ	↓ Δ	↓ Δ
Diagnostics performance	↑ ●	↓ Δ	↑ ●	↓ ●
Monitors	↑ ●	↓ Δ	↑ ●	↓ ●
— systems health	↑ ●	↓ Δ	↑ ●	↓ ●
— state	↑ ●	↓ Δ	↑ ●	↓ ●

↑ Industry meeting requirement

↓ Industry not meeting requirements

● Requirements stay the same

Δ Requirements increase

Primary investment priority

Secondary investment priority



## We welcome your feedback

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- ◆ We welcome feedback and suggestions for additional technology focus areas
- ◆ PathForward scope is potentially broader than outlined in the Project Description
- ◆ We anticipate multiple iterations and interactions with companies in the course of establishing PathForward development activities



# PathForward HomePage

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- ◆ ASCI PathForward Project Overview
- ◆ Request For Expression of Interest
- ◆ PathForward Project Description
  - This document describes the goals and technical rationale of the PathForward Project.
- ◆ ASCI PathForward Project Meeting
  - This document announces a Project Meeting being held on January 16, 1997.
- ◆ ASCI homepage
  - This webpage contains links to other ASCI projects and issues.
- ◆ ASCI Program Plan
  - This document provides a global overview of the ASCI program.
- ◆ Frequently Asked Questions (FAQ)